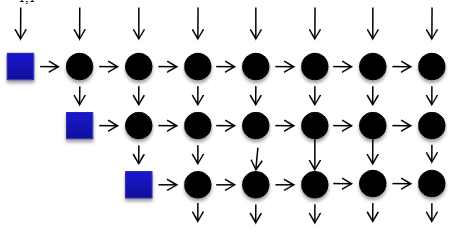
**ELEC 522 Assignment 5**

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# Description of QRD design architecture

 Here we adopted the design show in the slide. But with another row for easier control.

Each element can perform in either vectoring mode or rotating mode.

There will be additional unload input fed into the array for unloading.

# Model Composer model using the Vitis HLS block and testing results.

The screenshot shows the architecture of the QRD Array.

图示, 示意图

描述已自动生成

The following figure shows the test result on the example matrix. We can see that the result from the Simulink modules matched with theoretical results.

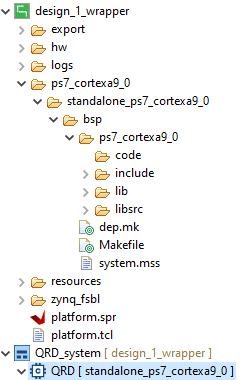
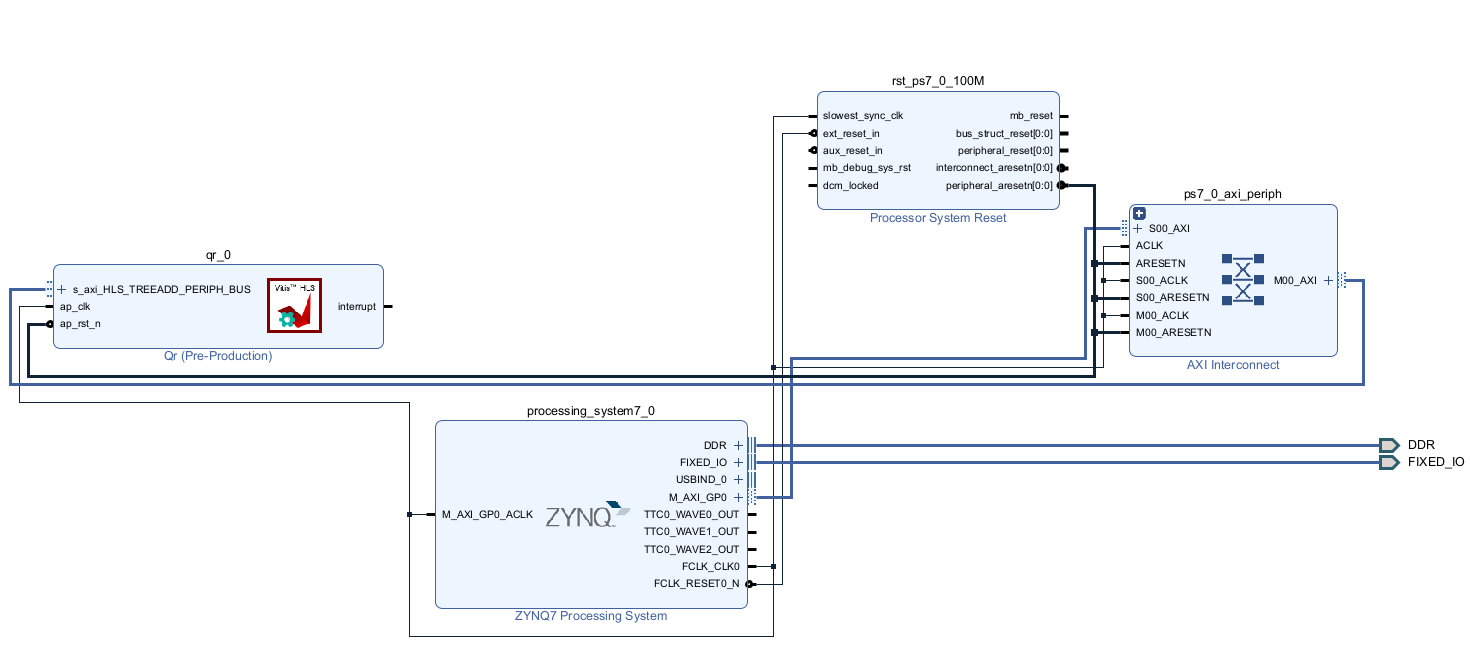
手机屏幕的截图

描述已自动生成文本

低可信度描述已自动生成

# Generate IP block from Model Composer and integrate with ARM processor using Vivado. Generate hardware and XSA for Vitis

The following two figure shows the Block Design Diagram in Vivado, and the compiled XSA in Vitis.

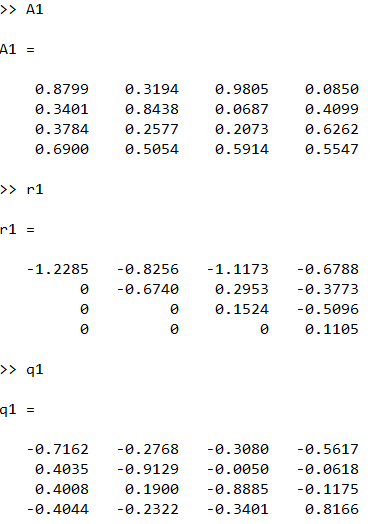
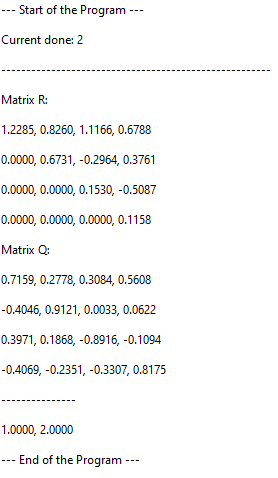


# Vitis C++ control of QRD Model Composer accelerator with testing results of at least 2 test matrices

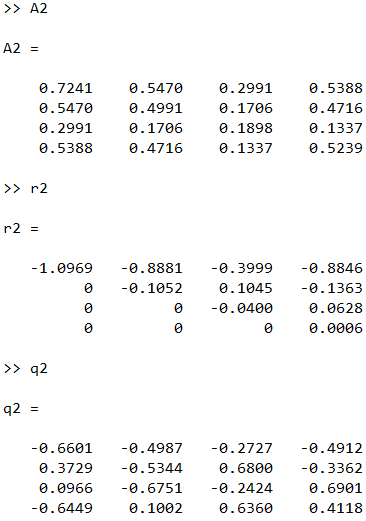
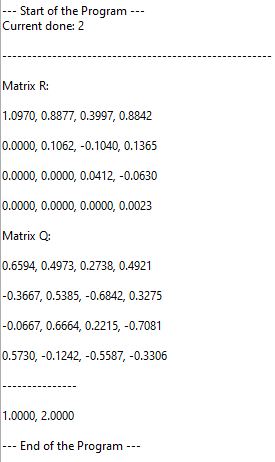
Note that the Q output by the program is the Q Transpose, so the results are correct. And in QR decomposition, the sign (+ / -) of Q and R are not important considering one flip in one row will be flipped back in another row during rotation, so we only need to compare the absolute value.

The following 4 screenshots show two test cases. The latter one may have a bit larger error, but that is due to the CORDIC iteration number and the cost brought by fixed point. The error is larger in the last row of Q in test case 2 compared to others, that is cost by the last row of R, we can see that R[4,4] in test case 2 is 0.006, which is very small. The last row of Q is generated by the last row of R, so the error will be larger too.

**Test Case 1**

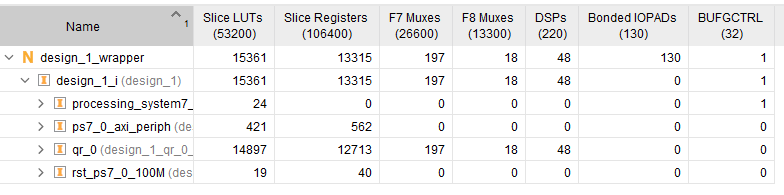
 

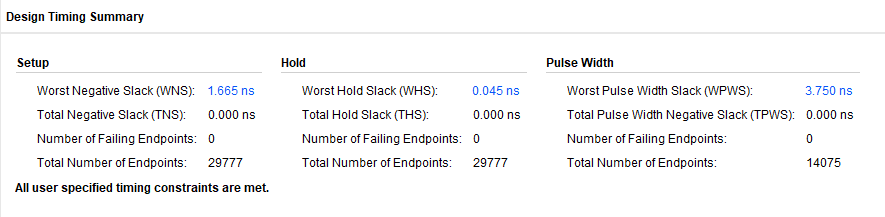
**Test Case 2**

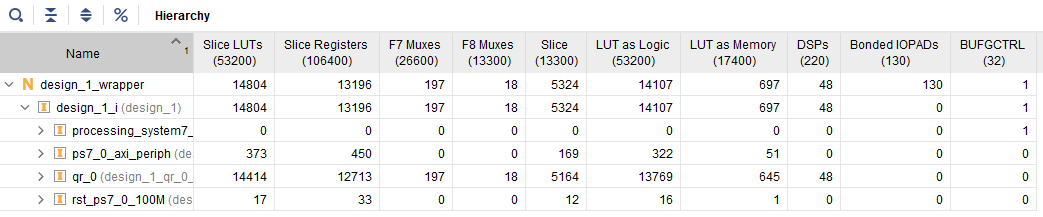
# Synthesis and place and route implementation report from Vivado.

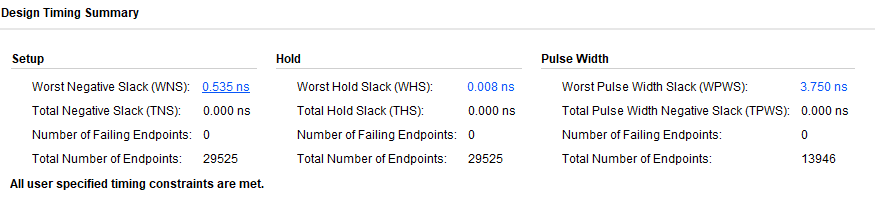
The following two figures are the area & timing report after synthesis.





The following two figures are the area & timing report after P&R.





# Turning in files including Model Composer file, screen capture of Vivado block diagram, Vitis C++ file, and screen capture of Vitis terminal results

All the screenshots are attached in this report.

* A5V3FIX > Vitis HLS files
* A5V3\_HDL > Vivado HDL project
* BareMetal > Vitis arm programs
* MATLAB > Model Composer files